CLAIMS

What is claimed is:

1. A processor comprising:
a plurality of registers;
a register renaming unit coupled to the plurality of registers to provide an architectural register file to store packed data operands, each of said packed data operands having a plurality of data elements;
a decoder, coupled to said register renaming unit, to decode a first and second set of instructions that each specify one or more registers in the architectural register file, each instruction in the first set of instructions specifying operations on all of the data elements stored in the specified one or more registers, each of the second set of instructions specifying an operation on only a subset of data element stored in a specified one or more registers; and
a partial-width execution unit, coupled to the decoder to execute operations specified by either of the first or the second set of instructions.

2. The processor of claim 1, wherein the subset of data elements stored in a specified one or more registers comprises corresponding least significant data elements.

3. The processor of claim 1, further comprising an execution unit to selectively perform a specified operation on one or more data elements

in the specified one or more registers depending upon which of the first or second set of instructions the specified operation is associated.

4. The procesor of claim 3, wherein the execution unit further comprises a plurality of multiplexers to select between a result of the specified operation and a predetermined value.

5. The processor of claim 3, wherein the execution unit further comprises a plurality of multiplexers to select between a data element of the one or more data elements and an identity function for input to the specified operation.

6. A method comprising the steps of:

receiving a single macro instruction specifying at least two logical registers in a packed data register file, wherein the two logical registers respectively store a first packed data operand and second packed data operand having corresponding data elements; and

independently operating on a first and second plurality of the corresponding data elements from said first and second packed data operands at different times using the same circuit to independently generate a first and second plurality of resulting data elements by

performing an operation specified by the single macro instruction on at least one pair of corresponding data elements in the first and second plurality corresponding

data elements to produce at least one resulting data element of the first and second plurality of resulting data elements, and

setting remaining resulting data elements of the first and second plurality of resulting data elements to one or more predetermined values, and

storing the first and second plurality of resulting data elements in a single logical register as a third packed data operand.

7. The method of claim 6, wherein the one or more predetermined values comprise values of data elements from either the first packed data operand or the second packed data operand.

8. The method of claim 6, wherein the one or more predetermined values comprise zero.

9. The method of claim 6, wherein the one or more predetermined values comprise a not-a-number (NaN) indication.